CCS Technical Documentation
RH-34 Series Transceivers

System Module

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Contents

Page No

Introduction 4
BB Hardware Characteristics 4
Technical Summary 4
Functional Description 5
Modes of Operation 5
RH-34 BB Functional Blocks 6
UEM and UPP 7
Battery 7
Charger Detection 10
Charger Interface Protection 10
LED Driver Circuit 11
LCD Display 12
RF Interface Block 13
Combo Memory Module 13
Combo Memory Interface 13
SRAM Memory Description 13
Flash Memory Description 13
Flash Architecture 14
Keyboard (UI Module) 14
Keyboard ESD Protection 14
Internal Audio 14
External Audio Connector 16
External Microphone Connection 17
External Earphone Connection 17
IrDa Interface 18
Vibra 18
FM Radio 18
System Connector (Tomahawk) 19
PWB Strategy 20
PWB Construction 20
PWB Immunity 21
Keyboard 21
Audio Lines 21
Microphone Lines 21
EAR Lines 22
Charger Lines 22
HEADINT 22
Battery Supply Filtering 22
System Connector 22
Mechanical Shielding 22
EMC Strategy 22
Test Interfaces 23
Production / After Sales Interface 23
Flash Interface 24
FBUS Interface 24
BB_RF Interface Connections 25

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RF Functional Description 27
Circuit Diagrams and PWB Layout 28
Receiver..... 28
Frequency Synthesizers..... 28
Transmitter 29
Antenna 31
Software Compensations 32
RF Frequency Plan..... 32
DC Characteristics..... 33

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Introduction

This document describes the system module for the RH-34 transceiver. The baseband module includes the baseband engine chipset, the UI components, and the acoustic components. RH-34 is a hand-portable dual band CDMA 850/1900 with AMPS. It has been designed using DCT4 generation baseband (UEM/UPP) and RF module. The baseband module has been developed as part of the DCT4 common Baseband. RH-34 contains some baseband features that are new to the America's CDMA market. These features include stereo FM receiver (offered as an accessory) and a MIDI (polyphonic ringing tones). The battery for RH-34 is the BLD-3 with a nominal capacity of 780 mAh.

BB Hardware Characteristics

- Hi-Resolution (128x128) illuminated color display
- Active LCD pixel area: width 27.6mm X height 27.6mm
- ESD-proof keymat, with five individual keys for multiple key pressing
- Support for internal semi-fixed battery (Janette type BLD-3)
- Audio amplifier and SALT speaker for MIDI support
- Ringing volume 100dB @ 5cm (MIDI tones through SALT speaker)
- Stereo FM receiver as an accessory
- IrDa port/interface
- Internal vibra
- Supports voice dial activation via headset button
- Six white LEDs for keymat on UI board and two for LCD backlight in LCD module
- 6-layer PWB, SMD with components on both sides of PWB

Technical Summary

The baseband module is implemented using two main ASICs — the Universal Energy Management (UEM) and the Universal Phone Processor (UPP). For detailed information on these two ASICs, see the *UEM ASIC Specification* and the *UPP8M_V1 ASIC Specification* documents. The baseband module also contains an audio amplifier for MIDI support and a 64-Mbit Flash/ 4-Mbit SRAM combo IC. EMC shielding is implemented using a metallized plastic frame. On the other side, the engine is shielded with PWB ground openings. Heat generated by the circuitry is conducted out via the PWB ground planes. The RH-34 transceiver module is implemented on six layer FR-4 material PWB.

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Functional Description

Modes of Operation

The RH-34 baseband engine has five different operating modes:

1 No supply

2 Acting Dead

3 Active

4 Sleep

5 Charging

No Supply Mode

In NO_SUPPLY mode, the phone has no supply voltage. This mode is due to the disconnection of the main battery or a low battery voltage level. The phone exits from NO_SUPPLY mode when a sufficient battery voltage level is detected. The battery voltage can rise either by connecting a new battery with VBAT > VMSTR+, or by connecting a charger and charging the battery voltage to above VMSTR+.

Acting DEAD Mode

If the phone powered off when the charger is connected, the phone is powered on and enters a state called Acting Dead. In this mode, no RF circuitry is powered up. To the user, the phone acts as if it is switched off. The phone issues a battery-charging alert and/or shows a battery charging indication on the display to acknowledge to the user that the battery is charging.

Active Mode

In active mode, the phone is in normal operation, scanning for channels, listening to a base station, transmitting, and processing information. There are several sub-states in the active mode depending on if the phone is in burst reception, burst transmission, etc. In active mode, SW controls the RF regulators by writing the correct values into the UEM control registers. VR1A/B and VR2 can be enabled or disabled. VR4 - VR7 can be enabled, disabled, or forced into low quiescent current mode. VR3 is always enabled in active mode.

Sleep Mode

The phone enters Sleep mode when both the MCU and the DSP are in stand-by mode. Both processors control sleep. When the SLEEPX low signal is detected, the UEM enters SLEEP mode. In this mode, the VCORE, VIO and VFLASH1 regulators are put into low quiescent current mode. All RF regulators — with the exception of VR2 and VR3 — are disabled in sleep mode. When the SLEEPX is set high and is detected by the UEM, the phone enters ACTIVE mode and all functions are activated. Sleep mode is exited either by the expiration of a sleep clock counter in the UEM, or by some external interrupt generated by a charger connection, key press, or headset connection among other things. While in

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sleep mode, the main oscillator is shut down and the baseband section uses the 32 kHz sleep clock oscillator as its reference.

Charging Mode

Charging can be performed in parallel with any other operating mode. The Battery Size Indicator (BSI) resistor inside the battery pack indicates the battery type/size. The resistor value corresponds to a specific battery capacity and technology. The UEM's AD converters, under UPP software control, measure the battery voltage, temperature, size, and current. The charging control circuitry (CHACON) inside the UEM controls the charging current delivered from the charger to the battery. The battery voltage rise is limited by turning the UEM switch off when the battery voltage has reached VBATLim (programmable charging cut-off limits 3.6V / 5.0V / 5.25V). Measuring the voltage drop across a 0.22Ohm resistor monitors charging current.

RH-34 BB Functional Blocks

RH-34 BB functional blocks are listed below:

- UEM and UPP
- Battery
- LED Driver
- LCD Display
- RF IF Block
- Memory Module
- Keyboard (UI module)
- External Audio Connector
- IrDa Interface
- Vibra
- FM Radio
- System Connector (Tomahawk)
- PWB Strategy
- EMC Strategy
- Test Interface

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UEM and UPP

The UEM contains a series of voltage regulators to supply both the baseband module and the RF module. Both the RF and Baseband modules are supplied with regulated voltages of 2.78 V and 1.8 V. The UEM contains six linear LDO (low drop-out) regulators for Baseband and seven regulators for RF circuitry. RF regulator VR1 uses two LDOs and a charge pump. VR1 regulator is used by RF module. The core of the UPP is supplied with a programmable voltage of 1.0 V, 1.3 V, 1.5 V, or 1.8 V. Note that with UEMK, VCORE supply voltage is set to 1.5 V. UEMC will support VCORE voltage below 1.5V.

The UPP operates from a 19.44MHz clock generated in the RF ASIC. The DSP and MCU both contain phase locked loop (PLL) clock multipliers, which can multiply the system frequency by factors from 0.25 to 31. The actual execution speed is limited by the memory configuration and process size (Max. DSP speed for C035 is ~ 200MHz).

The UEM contains a real-time clock, sliced down from the 32768 Hz crystal oscillator. The 32768 Hz clock is used by UPP as the sleep clock.

The communication between the UEM and the UPP is done via the bi-directional serial busses, CBUS and DBus. The CBUS is controlled by the MCU and operates at a speed of 1.08 MHz. The DBus is controlled by the DSP and operates at a speed of 13 MHz. Both processors are located in the UPP.

The interface between baseband and RF is implemented in the UEM and UPP ASIC. The UEM provides A/D and D/A conversion of the in-phase and quadrature receive and transmit signal paths. It also provides A/D and D/A conversions of received and transmitted audio signals to and from the user interface. The UEM supplies the analog signals to the RF section according to the UPP DSP digital control. The RF ASIC is controlled via the UPP RFBUS serial interface. There are also separate signals for PDM coded audio. Digital speech processing is handled by the DSP inside the UPP ASIC. The UEM is a dual voltage circuit with the digital parts running from the baseband supply (1.8V) and the analog parts running from the analog supply of 2.78V. The input battery voltage (VBAT) is also used directly by some UEM blocks.

The baseband supports both internal and external microphone inputs as well as speaker outputs. Input and output signal source selection and gain control is done by the UEM according to control messages from the UPP. Keypad tones, DTMF, and other audio tones are generated and encoded by the UPP and transmitted to the UEM for decoding. RH-34 has two external serial control interfaces: FBUS and MBUS provided by UEM. These busses can be accessed only through production test patterns.

RH-34 uses UPP8Mv2.4 and UEMK, with provision to use UEMC and future releases of UPP as it becomes necessary. UEMC requires some software changes.

Battery

BLD-3 Li-ion (inbox battery) is used as the main power source for RH-34. No other battery packs are planned to be used. BLD-3 has the capacity of 780 mAh.

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Table 1: BLD-3 characteristics

Description	Value
Nominal discharge cut-off voltage	3.1V
Nominal battery voltage	3.7V
Nominal charging voltage	4.2V
Maximum charger output current	850mA
Minimum charger output current	200mA
Cell pack impedance -20 ... 0 ^{o}C	180mΩ max
Cell pack impedance 0 ... +20 ^{o}C	150mΩ max
Cell pack impedance +20 ...+60 ^{o}C	130mΩ max
Cell pack impedance +60 ...+80 ^{o}C	250mΩ max

Table 2: Pin numbering of battery pack

Signal name	Pin number	Function
VBAT	1	Positive battery terminal
BSI	2	Battery capacity measurement (fixed resistor inside the battery pack)
BTEMP	3	Battery temperature measurement (measured by ntc resistor inside pack)
GND	4	Negative/common battery terminal

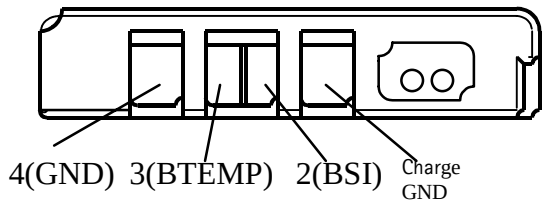

Figure 1: Battery pack contacts

The BSI fixed resistor value indicates type and default capacity of a battery. NTC-resistor measures the battery temperature.

Temperature and capacity information is needed for charge control. These resistors are connected to the BSI and BTEMP pins of the battery connector. Phone has 100 kW pull-up resistors for these lines so that they can be read by A/D inputs in the phone. For safety

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reasons, the phone software will shut the phone off if it senses a temperature of 38°C or higher on BTEMP line.

Table 3: BSI resistor values

Parameter	Min	Typ	Max	Unit	Notes
Battery size indicator resistor BSI		75		kΩ	Battery size indicator (BLD-3) Tolerance "1%
NTC thermistor BTEMP		47 4000		kΩ K	Battery temperature indicator (NTC pulldown) 47kΩ"5% @ 25 °C Beta value (B). Tolerance "5%, 25 °C / 85 °C

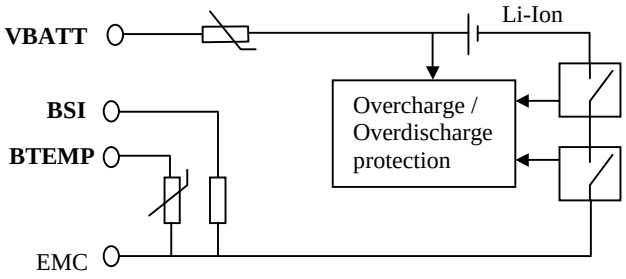

Figure 2: Interconnection diagram

Supply Voltage Regulation

The UEM ASIC controls supply voltage regulation. There are six separate regulators used by the baseband block. For a more detailed description about the regulator parameters, see the document *UEM ASIC Specification*.

Charging

RH-34 baseband supports the NMP charger interface specified in the document *Janette Charger interface*, SW control is specified in *EM SW Specification, ISA EM Core SW Project*. The UEM ASIC controls charging, and external components are used to provide EMC, reverse polarity, and transient protection of the charger input to the baseband module. The charger connection is through the system connector interface. Both 2- and 3-wire type chargers are supported. The operation of the charging circuit has been specified to limit the power dissipation across the charge switch and to ensure safe operation in all modes.

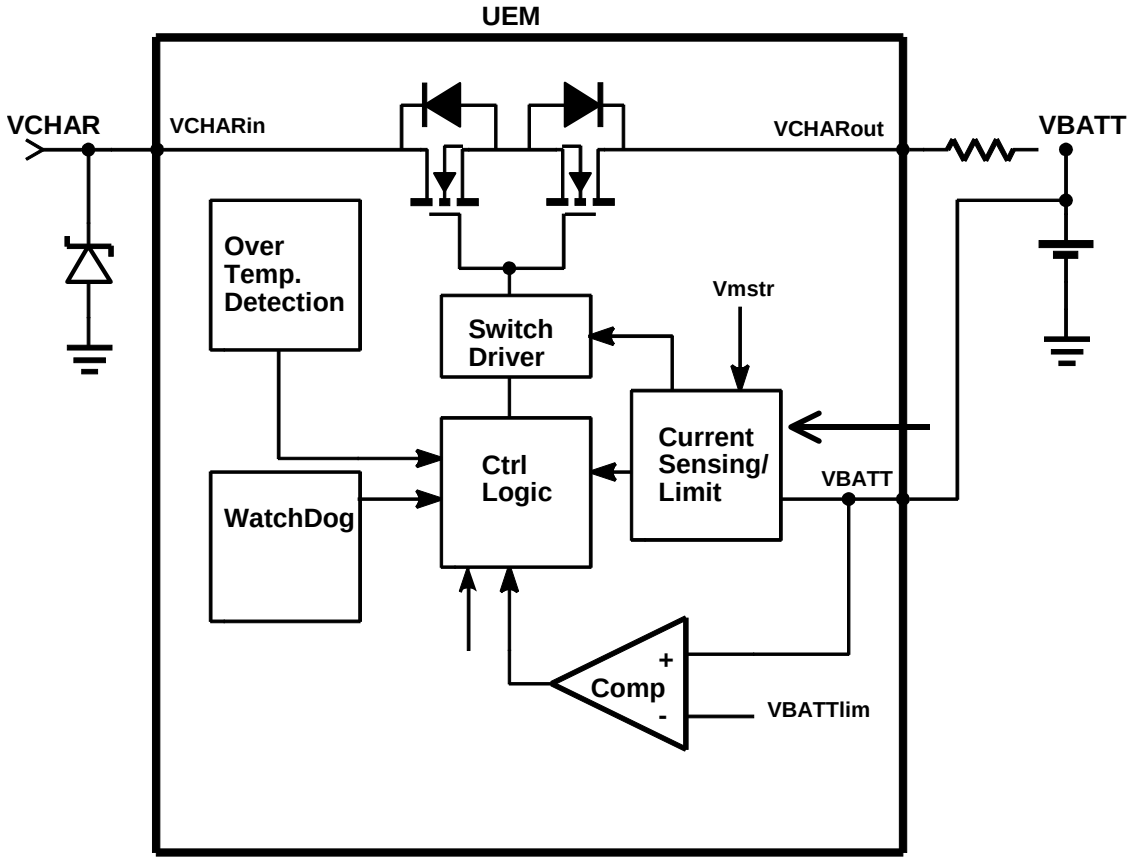

Figure 3: UEM charging circuitry

Charger Detection

Connecting a charger creates voltage on the VCHAR input to the UEM. When the VCHAR input voltage level rises above the VCHDET+ threshold, the UEM starts the charging process. VCHARDET signal is generated to indicate the presence of the charger for the SW.

Energy Management (EM) SW controls the charger identification and acceptance.

The charger recognition is initiated when the EM SW receives a "charger connected" interrupt. The algorithm basically consists of the following three steps:

1 Check that the charger output (voltage and current) is within safety limits.

2 Identify the charger.

3 Check that the charger is within the charger window.

If the charger is identified and accepted, the appropriate charging algorithm is initiated.

Charger Interface Protection

In order to ensure safe operation with all chargers and in mis-use situations, charger

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interface is protected using a transient voltage suppressor (TVS) and a 1.5A fuse. The TVS device used in RH-34 is rated for 16V@175W.

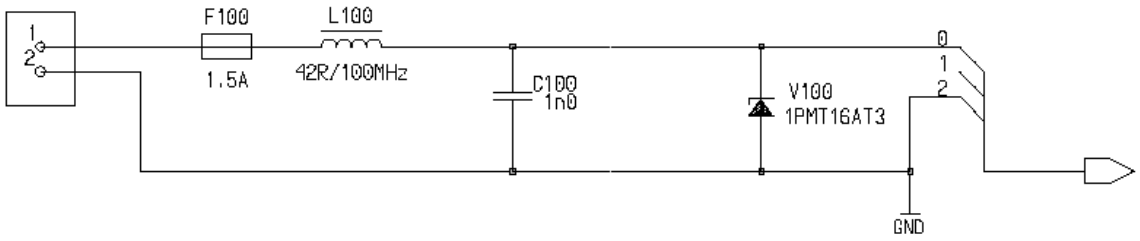

Figure 4: Charger interface TVS characteristics

Breakdown voltage (VBR)	17.8Vmin (at IT 1.0mA)
Reverse standoff voltage (VR) 1	6V
Max reverse leakage current at VR (IR)	5uA
Max peak impulse current (Ipp)	7A (at Ta=25*C, current waveform: 10/1000us)
Max clamping voltage at Ipp (Vc)	26V

LED Driver Circuit

In RH-34, white LEDs are used for LCD and keypad lighting. Two LEDs are used for LCD lighting and six are used for the keyboard. A step-up DC-DC converter (TK11851) is used as the white LED driver.

The display LEDs are driven in serial mode to achieve stable backlight quality. This means that constant current flows through LCD LEDs. Serial resistance Rlcd is used to define the proper current. The feedback signal, FB, is used to control the current. Driver increases or decreases the output voltage for LEDs to keep the current stable.

Keyboard LEDs are driven in 2-serial/3 parallel modes. Serial resistance R is used to limit the current through LEDs. The feedback signal, FB, is not used to control the current. Driver is controlled by the UEM via DLIGHT output. This signal is connected to driver EN-pin (on/off). It is possible to control the LED brightness by PWM to achieve smooth on/off operation.

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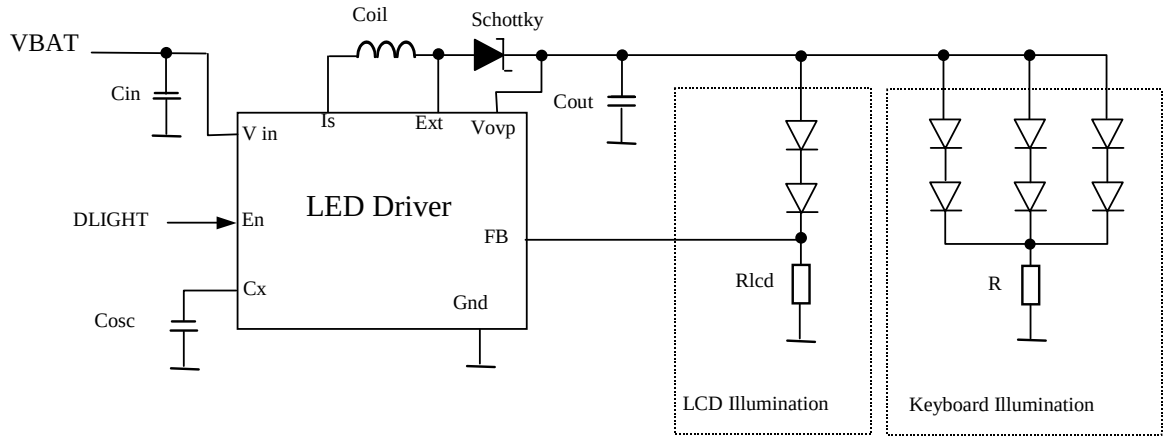

Figure 5: Shared LED driver circuit for LCD and keyboard backlight

LCD Backlight

LCD Backlight consists of two white LEDs, which are integrated with the LCD module.

Keyboard Illumination

The keyboard light consists of six white LEDs on the UI board. They are placed under the keyboard for proper illumination of the keypad.

LCD Display

The LCD is a CSTN 130 x 130, ful-dot matrix display with 12bit (4096 colors) color resolution and a single pixel border area around the content area, which makes the total active area 128 x 128 pixels.

Table 4: LCD general specifications

LCD parameter	Value
Glass size, width x height x thickness	33.98 mm x 37.95 mm x 1.71 mm
Glass thickness	0.50 mm
Viewing area (width x height)	30.29 mm x 30.29 mm
Active pixel area (width x height)	27.29 mm x 27.29 mm
Number of pixels	130 x 130 pixels
Technology	CSTN (color super twisted nematic)
Operating temperature range	-25 ^{o}C to +70 ^{o}C
Main viewing direction	6 o'clock
Illumination mode	transflective
Color tone Background:	Neutral/Black

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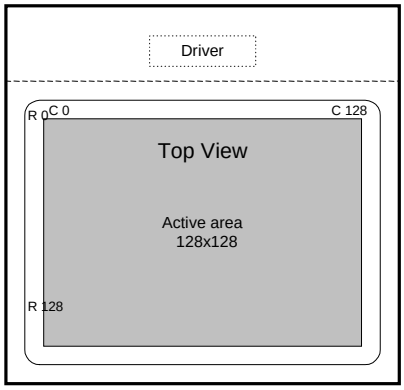

Figure 6: Color LCD module

RF Interface Block

The interface between the baseband and the RF module can be divided into two categories, the digital interface and the analog interface. The digital interface is between the UPP and the RF chip. The serial digital interface is used to control the operation of the different blocks in the RF chip. The analog interface is between the UEM and the RF.

Combo Memory Module

The RH-34 baseband memory module consists of a combo Flash/SRAM chip. It has 64Mbit burst-type flash memory and 4-Mbit of SRAM. In addition, the UPP has 8Mbit of internal RAM. The UPP RAM is part of the UPP and is not covered here.

Combo Memory Interface

The memory interface consists of multiplexed address/data bus MEMADDA [23:0], the MEMCONT[9:0] memory control bus, and GENIO[23] — which is used for memory control. The purpose of the memory interface is to reduce the amount of interconnections by multiplexing the address and data signals on the same bus. Because the required flash address space is more than 16-bits, the MEMADDA[15:0] are multiplexed address/data lines and MEMADDA[21:16] are only address lines, which in total allow for 4M addresses (MEMADDA[21:0]). The multiplexed data/address lines require the memory to store the address during the first cycle in the read/write access. Data access to the flash is performed as a 16-bit access (MEMADDA[15:0]) in order to improve the data rate on the bus. The memory interface supports asynchronous read, burst mode synchronous read, and simultaneous read-while-write/erase — all controlled by the UPP.

SRAM Memory Description

The combo memory chip used in RH-34 has 4 Mbit of SRAM, 16-bits wide running at 1.8V. It uses a multiplexed address and data bus to minimize the pin count of the device. Control signals are used to allow byte access to the device.

Flash Memory Description

The 64 Mbit density flash with 16-bit data access operates in both asynchronous random access and synchronous burst access (with crossing partition boundaries) and has various

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data protection features. Upon power up or reset, the device defaults to asynchronous read configuration. Synchronous burst read is indicated to the device by writing to the flash configuration register and can be terminated by deactivating the device.

The device supports reads and in-system erase and program operations at Vcc=1.8 V (Voltage range 1.7-1.9 V). Flashing at production is supported at Vpp=12 V (for limited exposure length only).

Flash Architecture

The datasheet of RH-34 combo memory contains detailed information about Flash architecture.

Keyboard (UI Module)

RH-34 consists of separate UI board and includes contacts for the keypad domes and LEDs for keypad lighting. The UI board is connected to the main PWB through a 16 pole board-to-board connector with springs. A 5x4-matrix keyboard is used in RH-34. Key pressing is detected by a scanning procedure. Keypad signals are connected via the UPP keyboard interface.

When no key is pressed, row inputs are high due to UPP internal pull-up resistors. The columns are written zero. When a key is pressed, one row is pulled down and an interrupt is generated to the MCU. After receiving the interrupt, the MCU starts the scanning procedure. All columns are first written high and then one column at a time is written down. All columns, except the column that is written down, are set as inputs. Rows are read while column at the time is written down. If a row is down, it indicates that key, which is at the cross point of the selected column and row that was pressed. After detecting the pressed key, all registers inside the UPP are reset and columns are written back to zero.

Keyboard ESD Protection

SMD chips LEDs on UI board have 2kV ESD protection. In case the A-cover is removed, there is a potential risk of damaging LEDs with electrostatic discharge. Ground openings are made around LEDs to catch ESD sparks. For additional protection, dome sheet is made of conductive metallized tape and grounded to display shield.

Internal Audio

Internal Microphone

The internal microphone capsule is mounted to in the UI frame. Microphone is omni directional and it's connected to the UEM microphone input MIC1P/N. The microphone input is asymmetric and the UEM (MICB1) provides bias voltage. The microphone input on the UEM is ESD protected. Spring contacts are used to connect the microphone to the main PWB.

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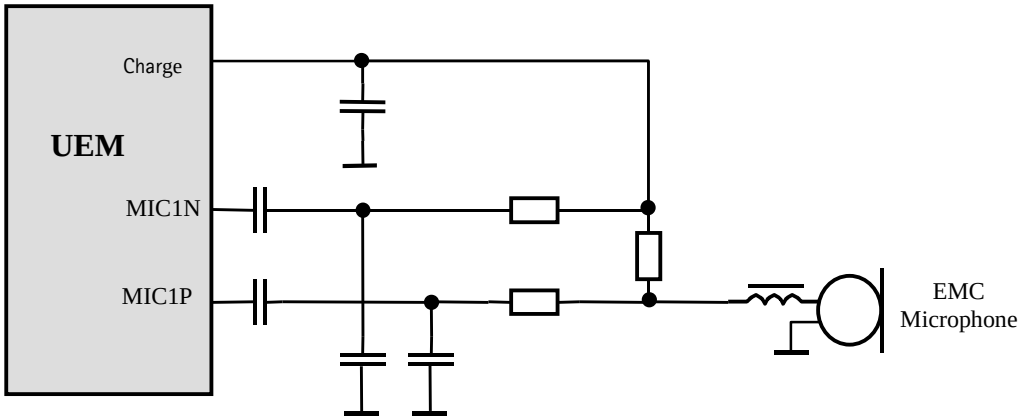

Figure 7: Internal microphone connection

Internal Speaker

The internal earpiece is a dynamic earpiece with impedance of 32 ohms. The earpiece is low impedance one since the sound pressure is to be generated using current and not voltage as the supply voltage is restricted to 2.7V. The earpiece is driven directly by the UEM and the earpiece driver (EARP and EARN outputs) is a fully differential bridge amplifier with 6 dB gain. In RH-34, 8mm leak tolerant PICO earpiece is used.

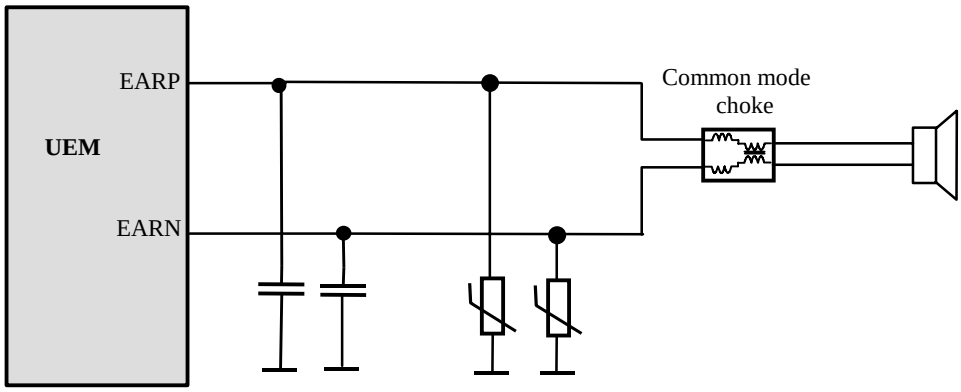

Figure 8: Speaker connection

IHF Speaker and Stereo Audio Amplifier

Integrated Hands Free Speaker (16mm MALT) is used to generate speech audio, ringing and warning tones in RH-34. Audio amplifier is controlled by the UPP. Speaker capsule is mounted in the C-cover. Spring contacts are used to connect the IHF Speaker contacts to the main PWB.

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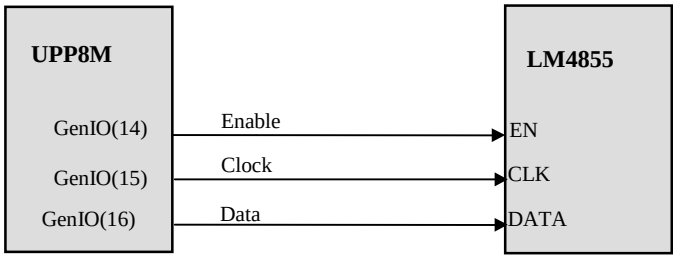

Figure 9: Digital interface of audio amplifer

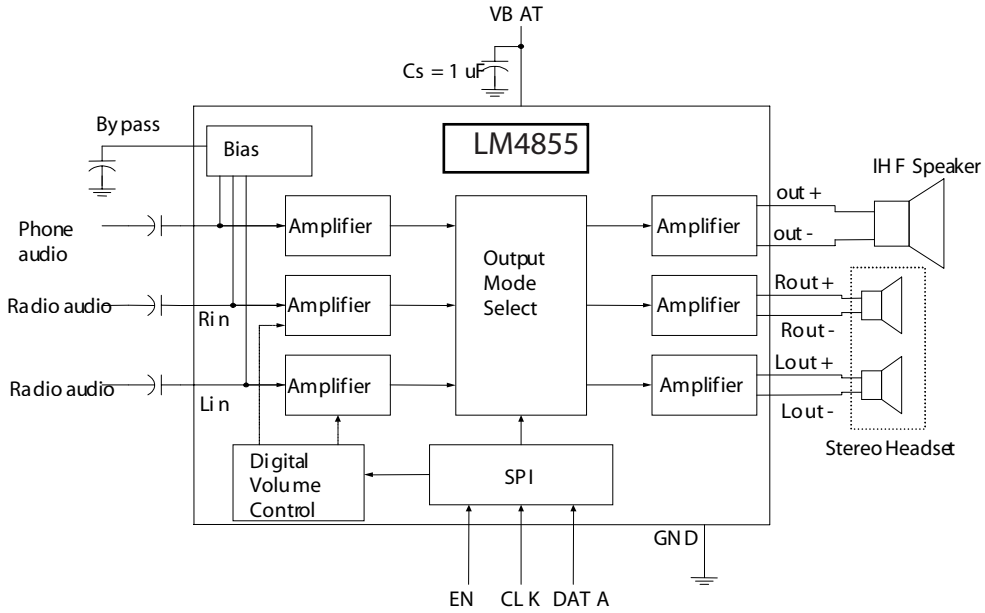

Figure 10: Block diagram of audio amplifer

The LM4855 features a 32-step digital volume control and eight distinct output modes. The digital volume control and output modes are accessed through a 3-wire interface, controlled by UPP. Digital volume control is needed when FM radio is activated; there is no amplifier block in FM radio module. Output modes are needed when routing audios to different locations; Headset or IHF.

External Audio Connector

RH-34 is designed to support fully differential external audio accessory connection by using Tomahawk system connector. Tomahawk connector has serial data bus called (ACI) Accessory Control Interface (ACI) for accessory insertion and removal detection and identification and authentication. ACI line is also used for accessory control purposes.

- 4-wire fully differential stereo audio (used also FM-radio antenna connection)
- 2-wire differential mic input

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External Microphone Connection

The external microphone input is fully differential and lines are connected to the UEM microphone input MIC2P/N. The UEM (MICB2) provides bias voltage. Microphone input lines are ESD protected.

Creating a short circuit between the headset microphone signals generates the hook signal. When the accessory is not connected, the UEM resistor pulls up the HookInt signal. When the accessory is inserted and the microphone path is biased the HookInt signal decreases to 1.8V due to the microphone bias current flowing through the resistor. When the button is pressed the microphone signals are connected together, and the HookInt input will get half of micbias dc value 1.1 V. This change in DC level will cause the HookInt comparator output to change state, in this case from 0 to 1. The button can be used for answering incoming calls but not to initiate outgoing calls.

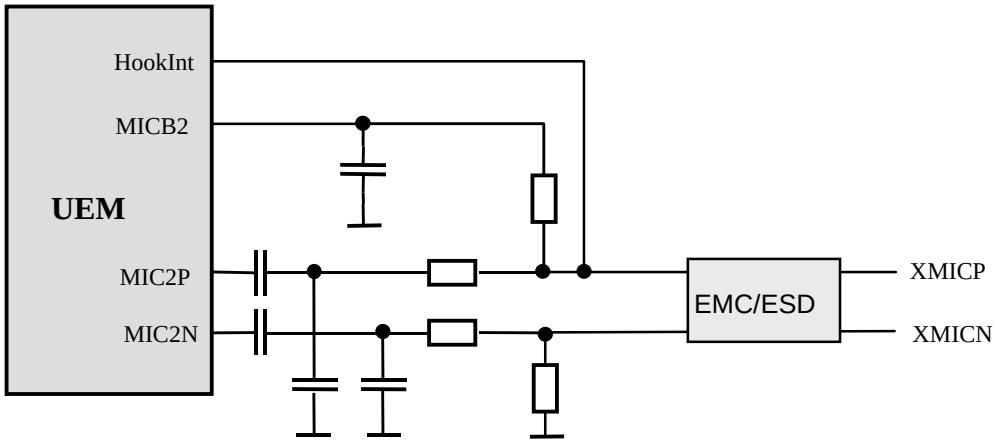

Figure 11: External microphone connection

External Earphone Connection

Headset implementation uses separate microphone and earpiece signals. The accessory is detected by the HeadInt signal when the plug is inserted.

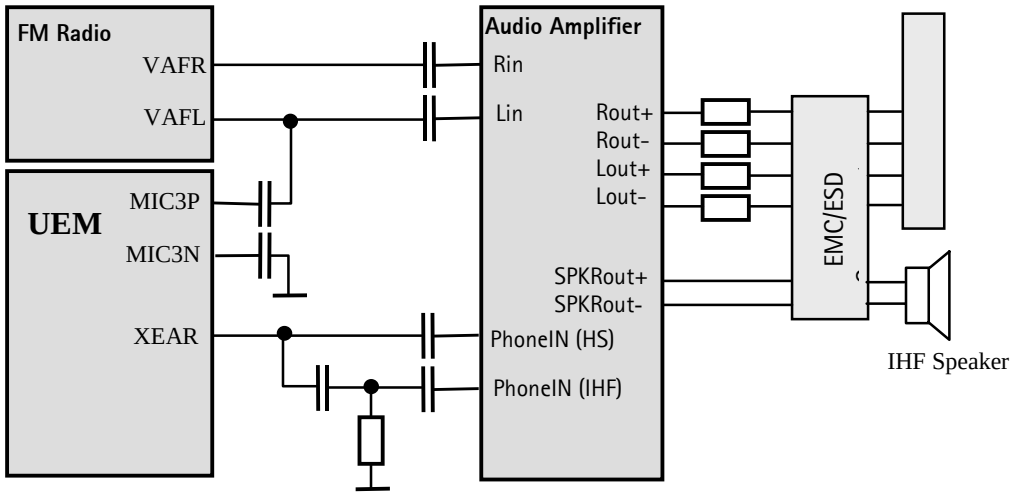

Figure 12: External earphone and IHF connections

IrDa Interface

The IrDa interface when using transceiver with 1.8V I/O is designed into the UPP. The IR link supports speeds from 9600 bit/s to 1.152 MBit/s up to distance of 80 cm. Transmission over the IR is half-duplex.

The length of the transmitted IR pulse depends on the speed of the transmission. When 230.4 kbit/s or less is used as a transmission speed, pulse length is maximum 1.63ms. If transmission speed is set to 1.152Mbit/s, the pulse length is 154ns.

IR transceiver can be set into SIR or MIR modes. In SIR mode transceiver is capable of transmission speed up to 115.2kbit/s. In MIR mode faster transmission speeds are used. The maximum speed is 1.152Mbit/s. IR transceiver can be set into shutdown mode by setting SD pin to logic '1' for current saving reasons.

Vibra

A vibra alerting device is used to generate a vibration signal for an incoming call. Vibra is located in the bottom end of the phone and connection is done with spring contacts. Vibra interface is the same like other DCT4 projects. The vibra is controlled by a PWM signal from the UEM. Frequency can be set to 64, 129, 258, or 520 Hz and duty cycle can vary between 3% - 97%. To ensure compatibility with different version of UEM, RH-34 uses 40.5% duty cycle of the vibra PWM signal.

FM Radio

FM radio circuitry is implemented by using highly integrated radio IC, TEA5767. TEA5767 is a single-chip, electronically tuned FM stereo radio with fully integrated IF selectivity and demodulation. The IF-frequency is 225 kHz. The radio is completely adjustment-free and does only require a minimum of small and low-cost external components. It has signal-dependent mono/stereo blend [Stereo Noise Cancelling (SNC)]. The radio can tune the European, US, and Japan FM bands. **This will be offered as an accessory with RH-34.**

Channel tuning and other controls are controlled through serial bus interface by the MCUSW. Reference clock, 32kHz, is generated by the UPP CTSI block (routed from sleep clock).

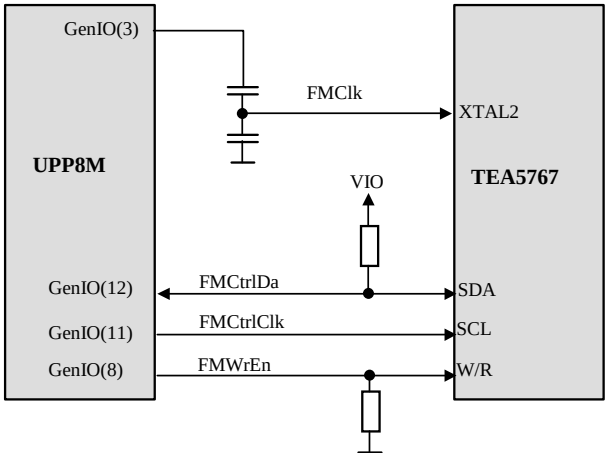

Figure 13: FM radio digital interface connections

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System Connector (Tomahawk)

The 14-pin Tomahawk bottom connector consists of charging plug socket and Tomahawk System Connector. Tomahawk system connector includes signals for the following:

Table 5: Tomahawk system connector signals

Function	Notes
Charging	Pads for 2-wire charging in cradles
Audio	4-wire fully differential stereo audio output 2-wire differential microphone input FM radio antenna connection
Power supply for accessories	2.78V/70mA output to accessories
ACI (Accessory Control Interface)	Accessory detection/removal and controlling
FBUS	Standard FBUS
DKU-5 (similar to USB) (optional)	Power in 5V in from DKU-5 cable

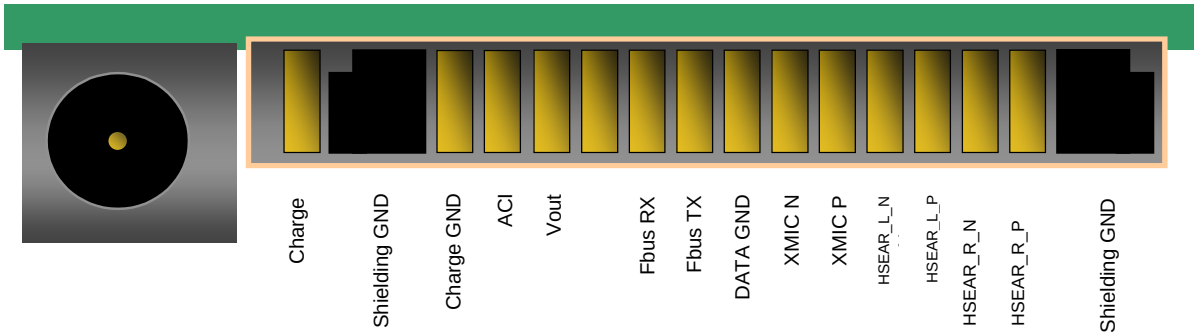

Figure 14: Tomahawk bottom connector (charger plug socket and Tomahawk system connector)

Accessory Control Interface (ACI)

ACI is point-to-point, bi-directional serial bus. It has three main features:

1 The insertion and removal detection of an accessory device

2 Acting as a data bus, intended mainly for control purposes

3 The identification and authentication of accessory type which is connected

The accessories are detected by the HeadInt signal when the plug is inserted. Normally when accessory is not present, the pull-up resistor 100k pulls up the HeadInt signal to VFLASH1. If the accessory is inserted, the external resistor (located to accessory) works as voltage divider and decreases the voltage level below the threshold of Vhead. Thereby the comparator output will be changed to high state causing an interrupt.

If the accessory is removed, the voltage level of HeadInt increases again to VFLASH1. This

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voltage level is higher than the threshold of the comparator and thereby its output will be changed to low. This changes is leading to an interrupt. These HeadInt interrupts are initiated the accessory detection or removal sequence.

External Accessory Regulator

An external LDO Regulator is needed for accessory power supply purposes. All ACI-accessories will require this power supply. Regulator input is connected to battery voltage VBAT and output is connected to Vout pin in Tomahawk connector. Regulator ON/OFF function is controlled via UPP.

The pull-down resistor on the enable input of the regulator is needed because in the switch-off mode of the phone, the output level of the Genio(0) is not defined. If Genio(0) is floating, the regulator may be enabled when it shouldn't be.

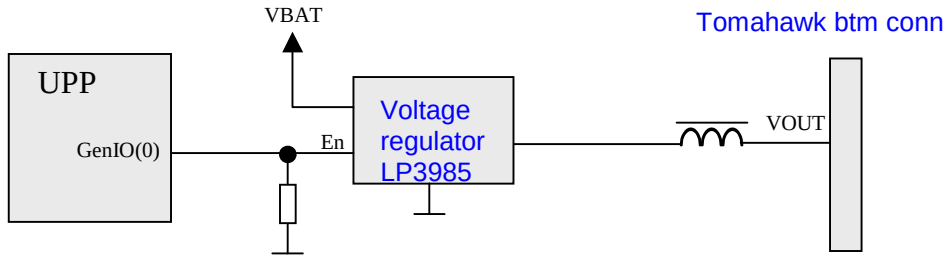

Figure 15: Accessory power supply diagram

PWB Strategy

PWB Construction

The PWB in RH-34 consists of a 6-layer board made up of FR4.

Via types are through hole, laser, buried, and blind vias.

The PWB build up is shown below:

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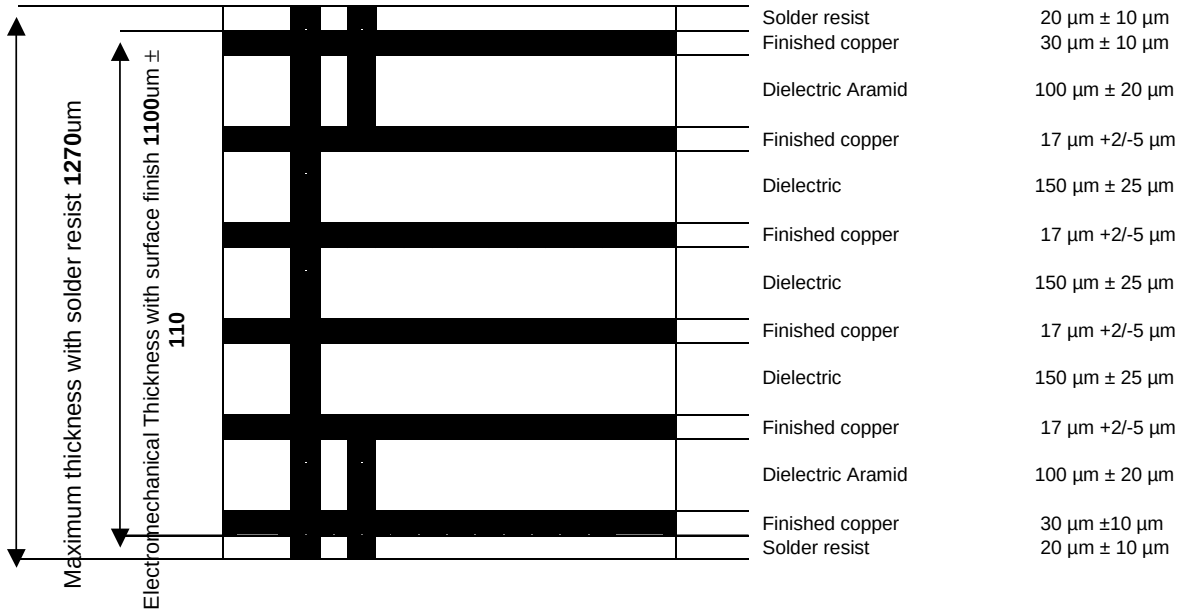
Maximum thickness with solder resist 1270um
Electromechanical Thickness with surface finish 1100um ± 110
Solder resist 20 µm ± 10 µm
Finished copper 30 µm ± 10 µm
Dielectric Aramid 100 µm ± 20 µm
Finished copper 17 µm +2/-5 µm
Dielectric 150 µm ± 25 µm
Finished copper 17 µm +2/-5 µm
Dielectric 150 µm ± 25 µm
Finished copper 17 µm +2/-5 µm
Dielectric 150 µm ± 25 µm
Finished copper 17 µm +2/-5 µm
Dielectric Aramid 100 µm ± 20 µm
Finished copper 30 µm ±10 µm
Solder resist 20 µm ± 10 µm

Figure 16: RH-34 PWB build up

PWB Immunity

The PWB has been designed to shield all lines susceptible for radiation. Sensitive PWB tracks have been drawn with respect to shielding by having ground plane over tracks, and ground close to the tracks at the same layer.

All edges are grounded from both sides of PWB and solder mask is opened from these areas. Target is that any ESD pulse faces ground area when entering the phone; for example, between mechanics covers. All holes in PWB are grounded and plated through holes.

Keyboard

The keyboard PWB layout consists of a grounded outer ring and either a trefoil pattern grid (matrix) or an inner pad. This construction makes the keys immune for ESD, as the keydome will have a low ohmic contact with the PWB ground.

Audio Lines

In order to obtain good signa-to-noise ratio and good EMC/ESD immunity, the audio lines have been carefully routed with respect to obtaining low impedance in the signal path and obtaining proper shielding.

Microphone Lines

Microphone signals are input lines and therefore very sensitive to radiated fields. Immunity for radiated fields is done to obtain a low-impedance path and with respect to a common noise point of view in the signal path. This is applied for both internal and external microphone lines.

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EAR Lines

EAR lines are output signals, also routed on layer 2 and 7, to obtain immunity for conducted emission from UEM. Internal EAR lines are EMC/ESD protected by radiated fields from the earpiece by the low-impedance signal path in the PWB.

The same PWB outline has been implemented for the SALT speaker. Low ohm coils inductors are used in series with the speaker for immunity against incoming fields from the speaker.

Charger Lines

Ground from the charger is connected directly to common PWB ground for low impedance path to the battery. The positive charger line will be ESD, EMC, and short-circuit protected by appropriate circuits.

HEADINT

This line is EMC/ESD protected by routing on shielded layer 2 and by placement of resistor R154 close to the bottom connector.

Battery Supply Filtering

Battery supply lines to the UEM IC are filtered with LC filter. These filters provide immunity against conducted RF noise

System Connector

The immunity strategy concerning the bottom connector lines is to shield all lines to this part in order to prevent radiation in the phone itself when external accessory is connected and to prevent radiated fields from disturbing the lines as well. Appropriate discrete filters close to the bottom connector are implemented for EMC and ESD protection.

Mechanical Shielding

RH-34 has metal shield over RF parts and BB parts to provide immunity for internal radiation and immunity for external fields.

EMC Strategy

The RH-34 phone must comply with the given CE requirements concerning EMC and ESD. The goal is to pass internal SPR requirements. Therefore attention has been paid to obtaining immunity in the PWB layout itself, and the implementation of filters in the circuit design.

Requirements for EMC and ESD:

- CE requirements for EMC and ESD according to ETS 300 342-1
- Internal requirements for EMC and ESD are according to SPR4

The baseband EMC strategy is divided into electrical and mechanical items. All electrical guide lines, clocks, and high-speed signals should be routed in inner layers and away from the PWB edges. Clock signals distributed to other circuits should have series resis-

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tors incorporated to reduce rise times and reflections. Slew rate controlled buffers should be used on custom components wherever possible to reduce the EMC produced by the circuit. Separate power supplies for digital, analog, and RF-blocks should be used as much as possible. Baseband and RF supply power rails should be isolated from each other by means of inductors in the power supply rail to prevent high-frequency components produced on the baseband power supply rail to spread out over the RF power supply plane. This might be required to avoid interference from digital circuits to affect the performance of RF section.

All external connectors and connection must be filtered using RC or LC networks to prevent the high frequency components from entering connection cables that then will act as antennas. The amount of this type of EMC component is in straight relation to the amount of external connections. The type of network and amount of components to be used is determined by the AC and DC impedance characteristic of that particular signal. Low-impedance signals require LC networks while medium impedance level signals (input signals at moderate bandwidth) can use RC networks.

The EMC protection should also prevent external or internal signals to cause interference to baseband and in particular to audio signals. Internal interference is generated by the transmitter burst frequency and the switchmode charging. The transmitter burst frequency interference is likely to cause noise to both microphone and earphone signals. The transmitter RF interference is likely to cause more problems in the microphone circuitry than in the earphone circuitry since the earpiece is a low impedance dynamic type.

As mechanical guidelines, the baseband and RF sections should be isolated from each other using EMC shielding, which suppresses radiated interference. The transmitter burst frequency can also generate mechanical vibrations that can be picked up by the microphone if it is not properly isolated from the chassis using rubber or some other soft material. Connection wires to internal microphone and earphone should be as short as possible to reduce the interference caused by internal signals.

ESD protection has to be implemented on each external connection that is accessible during normal operation of the phone.

Test Interfaces

Using the Tomahawk connector FBUS connections, the phone HW can be tested by PC software (i.e., Phoenix test software). In addition, RH-34 will also support Flash programming interface via the service battery, JTAG, and Ostrich test interfaces. JTAG test interface may be removed from the final product for security reasons.

Production / After Sales Interface

Test pads are placed on engine PWB, for service and production purposes. Same test pattern is used by the After Market Sales (AMS) group for product testing and software upgrades. The following figure shows the top view of the test pads. FBUS_TX and RX lines are used to transfer data in or out of the phone. VPP is the Flash programming voltage and MBUS/CLK line is used as Flash clock line during flashing of phone.

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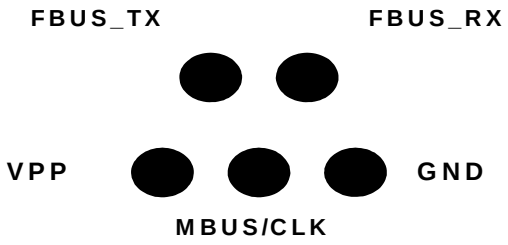

Figure 17: Production/test/after market interface

Flash Interface

Flash programming in production is done through the test pads in the above figure on the PWB.

FBUS Interface

FBUS is an asynchronous data bus having separate TX and RX signals. Default bit rate of the bus is 115.2 kbit/s. FBUS is mainly used for controlling and programming phone in the production. This is the primary interface used in RH-34.

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BB_RF Interface Connections

The BB and RF parts are connected together without a physical connector.

Rip #	Signal Name DAMPS, GSM1900	Connected from--- to		BB I/O		Signal Properties A/D--Levels---Freq./ Timing resolution		Description / Notes
RFICCNTRL(2:0)				**RF IC Control Bus from UPP to RF IC (TACO)**				
0	RFBUSCLK	UPP	RFIC	In	Dig	0/1.8V	9.72 MHz	RF Control serial bus bit clock
1	RFBUSDA	UPP/RFIC	RFIC UPP	I/O	Dig	(0: <0.4V 1: >1.4 V)		Bi-directional RF Control serial bus data,
2	RFBUSEN1X	UPP	RFIC	In	Dig			RFIC Chip Sel X
PUSL(2:0)				**Power Up Reset from UEM to RF IC (TACO)**				
0	PURX	UEM	RFIC	Out	Dig	0/1.8V	10us	Power Up Reset for RF IC
								SLCLK & SLEEPX not used in RF
GENIO(28:0)				**General I/O Bus connected to RF, see also separate collective GENIO(28:0) table. Control lines from UPP GENIOs to RF**				
5	TXP1	RFIC	UPP	Out	Dig	0/1.8V	10 us	Low Band Tx enabled
6	TXP2	RFIC	UPP	Out	Dig	0/1.8V		High Band Tx enabled
11	BANDSEL	**RFIC**	UPP	Out	Dig	0/1.8V		Rx Band select. Option for module LNA. **Not used in Stella.**

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Rip #	Signal Name DAMPS, GSM1900	Connected from--- to		BB I/O		Signal Properties A/D--Levels---Freq./ Timing resolution		Description / Notes
RFCLK (not BUS -> no rip #)				**System Clock From RF To BB, original source VCTCXO, buffered (and frequency shifted, WAM only) in RF IC (TACO)**				
	RFCLK	VCTCXO -> RFIC	UPP	In	Ana	800mVpp typ (FET probed) Bias DC blocked at UPP input	19.44 MHz	System Clk from RF to BB,
	RFClk GND	RF	UPP	In	Ana	0		System Clock slicer Ref GND, not separated from pwb GND layer
SLOWAD(6:0)				**Slow Speed ADC Lines from RF block**				
5	PDMID	RF Power detection module	UEM	In	Ana	0/2.7V dig	0/VR2	Power detection module identification to slow ADC (ch 5, previous VCTCXO Temp) signal to UEM.
6	PATEMP	RF Power detection module	UEM	In	Ana	0.1-2.7V	-	Tx PA Temperature signal to UEM, NTC in Power Detection Module
RFCONV(9:0)				**RF- BB differential Analog Signals: Tx I&Q, Rx I&Q and reference voltage**				
0	RXIP	RFIC	UEM	In	Ana	1.4Vpp max. diff. 0.5Vpp typ bias 1.30V		Differential positive/negative in-phase Rx Signal
1	RXIN							
2	RXQP							Diff. Positive/negative quadrature phase Rx Signal
3	RXQN							
4	TXIP	UEM	RFIC	Out	Ana	2.2Vpp max. diff. 0.6VppTyp Bias 1.30V		Differential positive/negative in-phase Tx Signal
5	TXIN							
6	TXQP							Differential positive/negative quadrature phase Tx Signal
7	TXQN							
9	VREFRFO1	UEM	RFIC	Out	Vref	1.35 V		RF IC Reference voltage from UEM

Rip #	Signal Name DAMPS, GSM1900	Connected from--- to		BB I/O		Signal Properties A/D--Levels---Freq./ Timing resolution		Description / Notes
RFAUXCONV(2:0)				**RF_BB Analog Control Signals to/from UEM**				
1	TXPWRDET	TXP Det.	UEM	In	Ana	0.1-2.4 V	50 us	Tx PWR Detector Signal to UEM
2	AFC	UEM	VCTCXO	Out	Ana	0.1-2.4 V		Automatic Frequency Control for VCTCXO

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VRF Globals instead of Bus				**Regulated RF Supply Voltages from UEM to RF. Current values are of the regulator specifications, not the measured values of RF**				
	VR1 A	UEM	RFIC	Out	Vreg	4.75 V +- 3 %	10 mA max.	UEM, charge pump + linear regulator output. Supply for UHF synth phase det ….
	VR1 B	UEM	RFIC	Out	Vreg	4.75 V +- 3 %	10 mA max.	UEM, charge pump + linear regulator output.
	VR2	UEM	RFDiscr./ RFIC	Out	Vreg	2.78 V +- 3 %	100 mA max.	UEM linear regulator. Supply voltage for Tx IQ filter and IQ to Tx IF mixer.
	VR3	UEM	VCTCXO	Out	Vreg	2.78 V +- 3 %	20 mA max.	UEM linear regulator. Supply for VCTCXO + RFCLK Buffer in RF IC.
	VR4	UEM	RFIC	Out	Vreg	--"--	50 mA max.	UEM linear regulator. Power Supply for LNA / RFIC Rx chain.
	VR5	UEM	RFIC	Out	Vreg	--"--	50 mA max.	UEM linear regulator. Power Supply for RF low band PA driver section.
	VR6	UEM	RFIC	Out	Vreg	--"--	50 mA max.	UEM linear regulator. Power supply for RF high band PA driver section.
	VR7	UEM	RFIC, UHF VCO	Out	Vreg	--"--	45mA	UEM linear regulator. Power supply for RF Synths
	IPA1	UEM	RF PA	Out	Iout	0-5 mA		Settable Bias current for RF PA L-Band
	IPA2	UEM	RFPA	Out	Iout	0-5 mA		Settable Bias current for RF PA H-band
	VFLASH1	UEM	RFIC	Out	Iout	2.78V	~2mA	UEM linear regulator common for BB. RFIC digital parts and RF to BB digi IF.
VBATT, Global								
	VBATTRF	Batt Conn	RFPA	Out	Vbatt	3…5V	0…1A 2A peak	Raw Vbatt for RF PA

RF Functional Description

Most of the RF functions are centered around RF ASIC. Receiver IF stages, low-band LNA, PLLs, RXVHF oscillator, TX VHF VCO active part and loop filter, high-band and low-band TX up-converters, TX IF stages, IQ modulator and demodulator and reference oscillator buffering are all integrated on single chip. RF design and sample testing are carried out by ASIC team. Application responsibility lies on RF design team as well as the components outside the RF ASIC. Externally sourced key components are:

- 19.44 MHz VCTCXO
- 2 GHz UHF VCO
- 800MHz PA
- 1900MHz PA
- Power detector module
- 1900MHz LNA transistor
- Duplexer low band

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- Duplexer high band
- RX800, RX1900, TX800, and TX1900 SAWs
- RX IF and TX IF Filters

The specifications for all key components are maintained by RF team and are available in network.

Circuit Diagrams and PWB Layout

Receiver

Receiver design and system partition come from Snoopy AD project. The receiver shows a superheterodyne structure with zero 2nd IF. Low-band and high-band receivers have separate front ends from diplexer to the 1st IF. Most of the receiver functions are integrated in RF ASIC. The only functions out of the chip are high-band LNA, duplexers, and SAW filters. In spite of a bit different component selection, receiver characteristics are very similar on both bands.

An active 1st down-converter sets naturally high gain requirements for preceding stages. Hence, losses in very selective front end filters are minimized down to the limits set by filter technologies used and component sizes. LNA gain is set up to 16dB, which is close to the maximum available stable gain from a single-stage amplifier. LNAs are not exactly noise matched in order to keep pass band gain ripple in minimum. Filters have relative tight stop band requirements, which are not all set by the system requirements but the interference free operation in the field. In this receiver structure, linearity lies heavily on mixer design. The 2nd order distortion requirements of the mixer are set by the 'half IF' suppression. A fully balanced mixer topology is required. Additionally, the receiver 3rd order IIP tends to depend on active mixer IIP3 linearity due to pretty high LNA gain.

IF stages include a narrowband SAW filter on the 1st IF and an integrated lowpass filtering is on zero IF. SAW filter guarantees 14dBc attenuation at alternating channels, which gives acceptable receiver IMD performance with only moderate VHF local phase noise performance. The local signal's partition to receiver selectivity and IMD depends then mainly on the spectral purity of the 1st local. Zero 2nd IF stages include most of receivers signal gain, AGC control range and channel filtering.

Receiver requirements and characteristics are presented in detail in RX specification.

Frequency Synthesizers

RH-34 synthesizer consists of three synthesizers: one UHF synthesizer and two VHF synthesizers. UHF synthesizer is based on integrated PLL and external UHF VCO, loop filter, and VCTCXO. It main goal is to achieve the channel selection, thus for dual band operations associated with dual mode. Due to the RX and TX architecture, this UHF synthesizer is used for down conversion of the received signal and for final up-conversion in transmitter. A common 2GHz UHFVCO module is used for operation on both low and high band. Frequency divider by two is integrated in the RF ASIC.

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Two VHF synthesizers consist of: RX VHF Synthesizer includes integrated PLL and VCO and loop filter and resonator. The output of RX-VHF PLL is used as LO signal for the second mixer in receiver. TX VHF Synthesizer and Loop filter is integrated into the RF ASIC. See depicted block diagrams and synthesizer characteristics from Synthesizer specification document.

Transmitter

The transmitter RF architecture is up-conversion type (desired RF spectrum is low side injection) with (RF-) modulation and gain control at IF. The IF frequency is 180.54MHz. The cellular band is 824.01-848.97MHz and PCS band is 1850.01-1909.95MHz.

Common IF

The RF modulator is integrated with Programmable Gain Amplifier (PGA) and IF output buffer inside RFIC-chip. I- and Q-signals, that are output signals from BB-side SW IQ-modulator, have some filtering inside the RF ASIC before RF modulation is performed. The required LO-signal from TXVCO is buffered with phase shifting in the RF ASIC. After modulation (p/4 DQPSK or FM), the modulated IF signal is amplified in PGA.

Cellular Band

At operation in cellular band, the IF signal is buffered at IF output stage that is enabled by TXP1 TX control. The maximum linear (balanced) IF signal level to 50W load is about -8 dBm.

For proper AMPS-mode receiver (duplex) sensitivity, IF signal is filtered in strip-filter before up-conversion. The upconverter mixer is actually a mixer with LO and output driver being able to deliver about +6dBm linear output power. Mixer is inside RF IC. Note, that in this point, term linear means -33dB ACP. The required LO power is about -6dBm. The LO signal is fed from RF IC.

Before power amplifier RF signal is filter in band filter. The typical insertion loss is about -2.7dB, and maximum less than -3.0dB. The input and output return losses are about -10dB.

Power amplifier is 50W/50W module. It does not have own enable/disable control signal, but it can be enabled by bias voltage and reference bias current signals. The gain window is +27 to +31dB and linear output power is +30dBm (typical condition) with -28dB ACP. The nominal efficiency is 50%.

PCS Band

At operation in PCS band, the IF signal is routed outside from RF IC to be filtered in TX IF strip filter, and after that back to RF IC, to the up-converter mixer. The LO-signal to the mixer is buffered and balanced inside RF IC. The mixer output is enabled by TXP2 TX control signal. The maximum linear (balanced) RF signal level to 50W load is about +7dBm.

After RF IC balanced RF-signal is single-ended in 1:1 balun and then filtered in SAW filter. The typical insertion loss is about -4.0dB, and maximum less than -5.0dB. This filter hasrelatively high pass band ripple about 1.0-1.5dB, largest insertion being at high end of the band. The input and return losses are about -10dB.

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Power amplifier is 50W/50W module. It does not have own enable/disable control signal, but it can be enabled by bias voltage and reference bias current signals. The gain window is +31 to +36dB and linear output power is +30dBm (typical condition) with -28dB ACP. The nominal efficiency is 40%.

Power Control

For power monitoring, there is a power detector module (PDM) build up from a (dual) coupler, a biased diode detector and an NTC resistor. RF signals from both bands are routed via this PDM. The RF isolation between couplers is sufficient not to loose filtering performance given by duplex filters.

The diode output voltage and NTC voltage are routed to BB A/D converters for power control purpose. The TX AGC SW takes samples from diode output voltage and compares that value to target value, and adjust BB I-and Q-signal amplitude and/or RF IC PGA settings to keep power control in balance.

NTC voltage is used for diode temperature compensation and for thermal shutdown when radio board's temperature exceeds +85°C.

False TX indication is based on detected power measurement when carrier is not on.

The insertion loss of coupler is -0.42dB (max) at cellular band and -0.48dB (max) at PCS band. Typical values for insertion losses are about -0.2dB. The filtering performance of diplexer is taken in account in system calculations.

Antenna Circuit

The antenna circuit stands for duplex filters and diplexer. The cellular band duplex filter is band pass type SAW filter with typical insertion loss about -2.0dB. The PCS band duplex filter is band stop (for receiver band) type ceramic filter and it's typical insertion loss is about -1.7dB. Insertion losses of diplexer are -0.45dB and -0.55dB (at maximum) for cellular and PCS band, typical values being about -0.30dB and -0.35dB.

RF Performance

The output power tuning target for power level 2 after diplexer (or after switch for external RF) is +27.3dBm for p/4 DQPSK type of modulation and +24.5dBm for FM type of modulation. Power levels downwards from PL2 are -4dB below next to highest power level, PL10 being -4.7dBm (and PL7 +6.5dBm with FM type of modulation). Modulation accuracy and ACP shall be within limits specified in IS-136/137.

Table 6: 800 MHz analog TX

Power level	RF power at external Antenna Pad (dBm)	Tuning target tolerant (dB)	Testing limits (dB)
2	24.8	+/- 0.25	0.5/-0.5
3	22.0	+/-0.5	+/-2.0
4	18.5	+/-0.5	+/-2.0

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Table 6: 800 MHz analog TX

Power level	RF power at external Antenna Pad (dBm)	Tuning target tolerant (dB)	Testing limits (dB)
5	14.5	+/-0.5	+/-2.0
6	10.5	+/-0.5	+/-2.0
7	6.5	+/-0.5	+/-2.0

Table 7: 800 MHz digital TX

Power level	RF power at external Antenna Pad (dBm)	Tuning target tolerant (dB)	Testing limits (dB)
2	27.3	+/- 0.25	0.5/-0.5
3	23.3	+/-0.5	+/-2.0
4	19.3	+/-0.5	+/-2.0
5	15.3	+/-0.5	+/-2.0
6	11.3	+/-0.5	+/-2.0
7	7.3	+/-0.5	+/-2.0
8	3.3	+/-0.5	+/-2.0
9	-0.7	+/-0.5	+/-2.0
10	-4.7	+/-0.5	+/-2.0

Table 8: CDMA 1900 TX

Power level	RF power at external Antenna Pad (dBm)	Tuning target tolerant (dB)	Testing limits (dB)
2	26.3***	+/- 0.25	0.5/-0.5
3	23.3	+/-0.5	+/-2.0
4	19.3	+/-0.5	+/-2.0
5	15.3	+/-0.5	+/-2.0
6	11.3	+/-0.5	+/-2.0
7	7.3	+/-0.5	+/-2.0
8	3.3	+/-0.5	+/-2.0
9	-0.7	+/-0.5	+/-2.0
10	-4.7	+/-0.5	+/-2.0

**** 26.3 dBm for channel 1000 and 1998; 27.0 dBm for channel 2.*

Antenna

The RH-34 antenna solution is an internal dual-resonance PIFA antenna. This antenna

has a common feeding point for both antenna radiators, which results in the need for diplexer. In a singleband transciever, a SMD-compatible through chip can be used.

Software Compensations

The following software compensations are required:

- Power levels temperature compensation
- Power levels channel compensation
- Power level reduction due to low battery Voltage
- TX Power Up/Down Ramps
- PA's bias reference currents vs. power, temp and operation mode
- RX IQ DC offsets
- RSSI channel compensation
- RSSI temperature compensation

RF Frequency Plan

The RH-34 frequency plan is shown in the following figure. A 19.44 MHz VCTCXO is used for UHF and VHF PLLs and as a baseband clock signal. All RF locals are generated in PLLs.

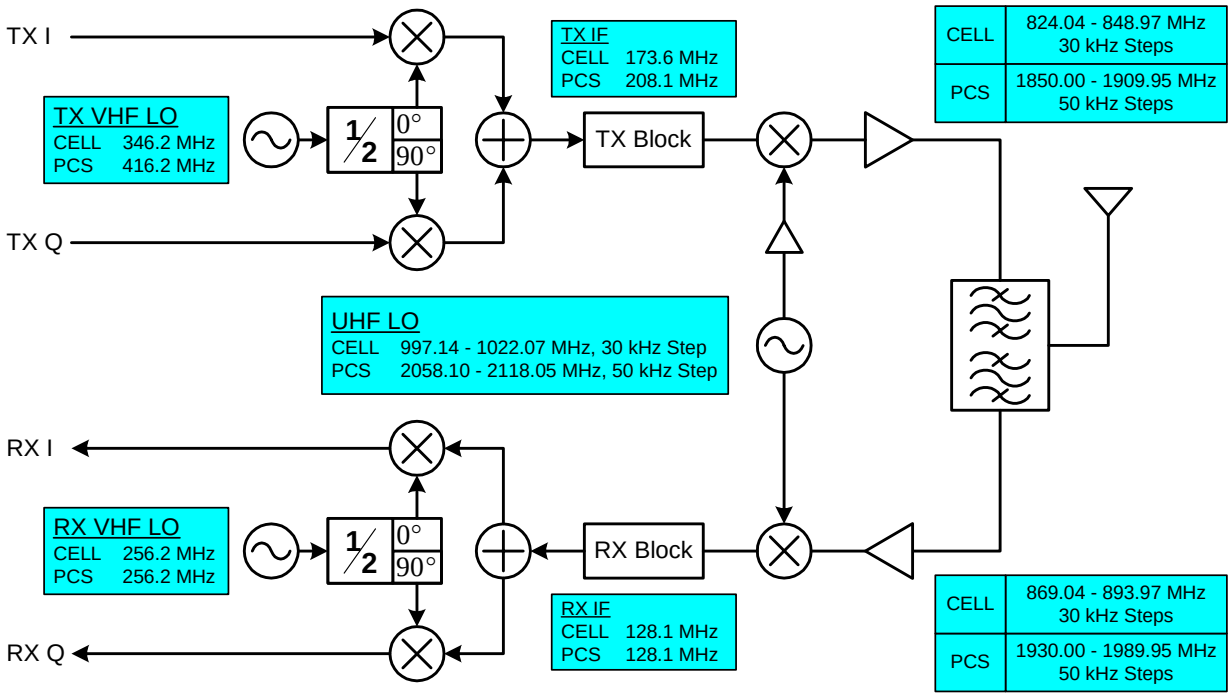

Figure 18: RH-34 frequency plan

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DC Characteristics

Regulators

The regulator circuit is UEM and the specifications can be found from:

Table 9: Regulator circuit information

Regulator name	Output voltage (V)	Regulator Max current (mA)	RF total 1GHz	RF total 2GHz
VR1 a/b	4.75 +/- 3%	10	4	4
VR2	2.78 +/-3%	100	100	76
VR3	2.78 +/-3%	20	2	2
VR4	2.78 +/-3%	50	23	24
VR5	2.78 +/-3%	50	5	0
VR6	2.78 +/-3%	50	tbd	tbd
VR7	2.78 +/-3%	45	40	45
IPA1, IPA2	2.7 max	1 +/- 10% 3 +/- 4% 3.5 +/- 4% 5 +/- 3%	1.3 - 5.0	1.3 - 3.7
VREFRF01	1.35 +/- 0.5%	0.12	0.05	0.05
VFLASH1	2.78 +/- 3%	70	1	1

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